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NOTICE OF ALLOWANCE AND FEE(S) DUE

48062 7590 04/28/2008

RYAN, MASON & LEWIS, LLP
1300 POST ROAD
SUITE 205
FAIRFIELD, CT 06824

EXAMINER

GANDHIL, DIPAKKUMAR B

ART UNIT

PAPER NUMBER

2117

DATE MAILED: 04/28/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,549	08/19/2003	Daniel R. Knebel	YOR920030213US1	4265

TITLE OF INVENTION: FREQUENCY MODIFICATION TECHNIQUES THAT ADJUST AN OPERATING FREQUENCY TO COMPENSATE FOR AGING ELECTRONIC COMPONENTS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1440	\$300	\$0	\$1740	07/28/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

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If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,549	08/19/2003	Daniel R. Knebel	YOR92030213US1	4265

TITLE OF INVENTION: FREQUENCY MODIFICATION TECHNIQUES THAT ADJUST AN OPERATING FREQUENCY TO COMPENSATE FOR AGING ELECTRONIC COMPONENTS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1440	\$300	\$0	\$1740	07/28/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
GANDHI, DIPAKKUMAR B	2117	714-746000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
<input type="checkbox"/> Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.	1_____
<input type="checkbox"/> "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE _____

(B) RESIDENCE: (CITY AND STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

4a. The following fee(s) are submitted:	4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
<input type="checkbox"/> Issue Fee	<input type="checkbox"/> A check is enclosed.
<input type="checkbox"/> Publication Fee (No small entity discount permitted)	<input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.
<input type="checkbox"/> Advance Order - # of Copies _____	<input type="checkbox"/> The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)	<input type="checkbox"/> a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.	<input type="checkbox"/> b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).
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Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS; SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,549	08/19/2003	Daniel R. Knebel	Y0R9 20030213US1	4265
48062	7590	04/28/2008		EXAMINER
RYAN, MASON & LEWIS, LLP 1300 POST ROAD SUITE 205 FAIRFIELD, CT 06824				GANDHIL DIPAKKUMAR B
				ART UNIT 2117 PAPER NUMBER
				DATE MAILED: 04/28/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 391 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 391 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/643,549	KNEBEL ET AL.	
	Examiner	Art Unit DIPAKKUMAR GANDHI	2117

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTO-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to 01/16/2008.

2. The allowed claim(s) is/are 1-28.

3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some* c) None of the:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

(a) including changes required by the Notice of Draftperson's Patent Drawing Review (PTO-948) attached 1) hereto or 2) to Paper No./Mail Date _____.

(b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- 1. Notice of References Cited (PTO-892)
- 2. Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3. Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____
- 4. Examiner's Comment Regarding Requirement for Deposit
of Biological Material
- 5. Notice of Informal Patent Application
- 6. Interview Summary (PTO-413),
Paper No./Mail Date _____.
- 7. Examiner's Amendment/Comment
- 8. Examiner's Statement of Reasons for Allowance
- 9. Other _____.

/Jacques Louis-Jacques/, AU 2117, 4/23/08

Allowable Subject Matter

1. Applicant's Appeal Brief filed on 01/16/2008 has been entered.
2. Applicant's arguments, filed 01/16/2008, with respect to the claims have been fully considered and are persuasive. The rejection of 10/17/2007 has been withdrawn.
3. Claims 1-28 are allowed.
4. The following is an examiner's statement of reasons for allowance:

The present invention relates to electronic systems and, more particularly, relates to frequency regulation for electronic components of the electronic systems.

The claimed invention (claim 1 as representative) recites features such as: "...the one or more performance parameters correlated with maximum operating frequency of one or more electronic components of the electronic system for the particular age of the electronic system".

The prior art of record (Maguire, Jr. et al.) teach a modeling system that arranges the model in a hierarchical structure of communicating and independently executing object modules controlled by an overall supervisor. Each object represents a component or a system and includes an object controller which communicates with other object modules, an object error checker and an object model (abstract, Maguire, Jr. et al.).

Norman et al. (US 5,956,289) teach an integrated circuit is described which has circuitry to detect environmental conditions such as temperature and supply voltage and adjust the operation of the circuit accordingly. A flash memory system is described which includes a temperature detector and a supply voltage detector (abstract, Norman et al.).

Morgan (US 6,525,603 B1) teaches a feedforward amplifier is linearized by adapting off the detection of an applied modulation source. The feedforward amplifier has two loops: a first loop and a second loop. Modulators in the two loops are adjusted by controllers that adapt in response to detection of the modulation source injected into the first loop (abstract, Morgan).

Wu et al. (Bipolar Bootstrapped Multi-emitter BiCMOS (B2M-BiCMOS) Logic for Low-Voltage Applications, Electronics, Circuits, and Systems, 1996, Volume 2, Pages: 1174-1177) teach to compare

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speed performance of the new BiCMOS logic circuit with those of CMOS, conventional BiCMOS, and Bootstrapped BiCMOS (BS-BiCMOS) logic circuits (abstract, Wu et al.).

Chur (US 5,124,849) teaches a method for detecting aberrations in a digital data storage medium, such as a magnetic media disk. In a media certifier, a series of signal pulses is produced by reading data previously written to a medium is examined for differential variations between each signal pulse and at least one other of those signal pulses in the local area of the medium (abstract, Chur).

Ohie et al. (US 5,936,448) teach an integrated circuit in which Schmitt input circuits can be tested in a short time and a highly accurate test result can be obtained. The integrated circuit includes switches each passing outputs of Schmitt inverters with inputs connected to input-output ports to the inputs of tristate circuits with outputs connected to adjacent input-output ports (abstract, Ohie et al.).

Burns et al. (US 4,698,587) teach a method for characterizing critical timing paths and analyzing timing related failure modes in high clock rate photocurrent at the drain of a single transistor in a very large scale integrated circuit (abstract, Burns et al.).

Hacker (US 4,845,419) teaches that in a system including volatile memory, a battery backed memory may be available for preserving data in the event of a power failure. Low power condition is reliably sensed sufficiently in advance of supply voltage falling below a minimum operating voltage range so as to give an adequate time interval, e.g. 2.5 milliseconds for the saving of application operating system status (abstract, Hacker).

Bassett et al. (US 5,127,008) teach a method and apparatus for designing very large scale integrated circuit devices, most particularly level sensitive scan design (LSSD) devices, by inclusion of a plurality of distributed delay lines originating at input terminals of the device, and controlling the inhibiting and enabling of driver circuits connected to the output terminals of the device, as required to regulate operation of device drivers during a plurality of testing operations (abstract, Bassett et al.).

Kolanek (US 2002/0047745 A1) teaches an amplifier subsystem has a modulator to generate a pair of constant amplitude phase-modulated components which are in response to an input signal, a pair of channels that include a pair of power amplifiers to amplify the components, and a combiner to combine the amplified components (abstract, Kolanek).

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Iida et al. (US 6,525,585 B1) teach a fixed-length delay generation circuit comprises a first variable delay circuit (VDC), a clock generation circuit, a VDC group including one or more second VDCs, and a delay controller (abstract, Iida et al.).

Takahashi (US 6,253,358 B1) teaches an overall calculation of a semiconductor integrated circuit comprising an assemblage of a plurality of circuit blocks is predicted at an initial stage of design (abstract, Takahashi).

The prior arts however do not teach the one or more performance parameters correlated with maximum operating frequency of one or more electronic components of the electronic system for the particular age of the electronic system.

Hence, the prior arts of record do not anticipate nor render obvious the claimed invention. Thus, claim 1 is allowable over the prior arts of record. Claims 2-19 are allowed because of the combination of additional limitations and the limitations listed above.

- Claim 20 recites similar features as in claim 1. Thus claim 20 is allowable over the prior arts of record. Claims 21-27 are allowed because of the combination of additional limitations and the limitations listed above.
- Claim 28 recites similar features as in claim 1. Thus claim 28 is allowable over the prior arts of record.
- Thus, claims 1-28 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to DIPAKKUMAR GANDHI whose telephone number is (571)272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JACQUES H LOUIS-JACQUES/
Supervisory Patent Examiner, Art Unit 2117

/Dipakkumar Gandhi/
Examiner, Art Unit 2117